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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/925,889	08/06/2001	Rasekh Rifaat	A0312/7412 WRM/IB	6192

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WOLF GREENFIELD & SACKS, PC
FEDERAL RESERVE PLAZA
600 ATLANTIC AVENUE
BOSTON, MA 02210-2206

EXAMINER	
BURD, KEVIN MICHAEL	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 03/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/925,889	RIFAAT ET AL.	
	Examiner	Art Unit	
	Kevin M. Burd	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 16-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 16-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. This office action, in response to the remarks submitted after final on 2/21/2006, is a final office action.

2. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Response to Arguments

3. Applicant's arguments, see the remarks filed 2/21/2006, with respect to the rejections of the claims under 35 USC 102(e) have been fully considered and are persuasive. Therefore, the rejections have been withdrawn. However, upon further consideration, new grounds of rejection are made in view of Agrawal et al (US 6,879,576) and Catherwood (US 6,934,728).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-14 and 16-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agrawal et al (US 6,879,576) and Catherwood (US 6,934,728).

Regarding claim 1, Agrawal discloses a method for processing signal values in a digital signal processor (column 16, lines 34-45). The processing units can be

implemented with a general purpose or specifically designed processor operated to execute instruction codes that achieve the functions described herein (column 16, lines 40-43). The processing units include multipliers 814 and accumulators 816 (column 16, lines 34-37). The multipliers and accumulators are complex (column 10, lines 56-62). The receiver of figure 7 receives the complex despreading code and data. The spreading code is discloses in column 7, line 64 to column 8, line 6. Agrawal does not disclose the complex multiplication, complex addition and storing of the despread result are executed in a single clock cycle of the DSP. However, Catherwood discloses a method for complex multiplication and accumulating a signal (abstract) and executing instructions which operate on data and write the results to an accumulator and write prior results to memory within a single processor cycle (column 5, line 65 to column 6, line 6). It would have been obvious for one of ordinary skill in the art at the time of the invention to implement the method of Agrawal in the single processor cycle of Catherwood. It is advantageous to implement functions of a processor in the shortest amount of time possible so results are available as quickly as possible.

Regarding claim 2, Agrawal discloses the accumulators 816 as stated above.

Regarding claim 3, Agrawal discloses the despreading code shown in figure 5 has a spreading factor divisible by four.

Regarding claims 4 and 5, Agrawal discloses the despreading code contains code segments comprising real and imaginary bits in figure 4.

Regarding claims 6 and 7, Agrawal discloses the channel bits shown in figures 4A and 4B.

Regarding claim 8, Agrawal discloses a method of calculating a data set in a digital signal processor (column 16, lines 34-45). The processing units can be implemented with a general purpose or specifically designed processor operated to execute instruction codes that achieve the functions described herein (column 16, lines 40-43). The processing units include multipliers 814 and accumulators 816 (column 16, lines 34-37). The multipliers and accumulators are complex (column 10, lines 56-62). The receiver of figure 7 receives the complex despreading code and data. The spreading code is discloses in column 7, line 64 to column 8, line 6. Agrawal does not disclose the complex multiplication, complex addition and storing of the despread result are executed in a single clock cycle of the DSP. However, Catherwood discloses a method for complex multiplication and accumulating a signal (abstract) and executing instructions which operate on data and write the results to an accumulator and write prior results to memory within a single processor cycle (column 5, line 65 to column 6, line 6). It would have been obvious for one of ordinary skill in the art at the time of the invention to implement the method of Agrawal in the single processor cycle of Catherwood. It is advantageous to implement functions of a processor in the shortest amount of time possible so results are available as quickly as possible.

Regarding claim 9, Agrawal discloses the accumulators 816 as stated above.

Regarding claim 10, Agrawal discloses the despreading code shown in figure 5 has a spreading factor divisible by four.

Regarding claims 11 and 12, Agrawal discloses the despreading code contains code segments comprising real and imaginary bits in figure 4.

Regarding claims 13 and 14, Agrawal discloses the channel bits shown in figures 4A and 4B.

Regarding claim 16, Agrawal discloses a digital signal processor (column 16, lines 34-45). The processing units described herein (e.g. multipliers, accumulators, pilot processors, data recovery element, controller and others) can be implemented in various manners such as on a DSP (column 16, lines 34-40). The DSP implements a method for processing signal values in a digital signal processor (column 16, lines 34-45). The processing units can be implemented with a general purpose or specifically designed processor operated to execute instruction codes that achieve the functions described herein (column 16, lines 40-43). The processing units include multipliers 814 and accumulators 816 (column 16, lines 34-37). The multipliers and accumulators are complex (column 10, lines 56-62). The receiver of figure 7 receives the complex despreading code and data. The spreading code is discloses in column 7, line 64 to column 8, line 6. Agrawal does not disclose the complex multiplication, complex addition and storing of the despread result are executed in a single clock cycle of the DSP. However, Catherwood discloses a method for complex multiplication and accumulating a signal (abstract) and executing instructions which operate on data and write the results to an accumulator and write prior results to memory within a single processor cycle (column 5, line 65 to column 6, line 6). It would have been obvious for one of ordinary skill in the art at the time of the invention to implement the method of Agrawal in the single processor cycle of Catherwood. It is advantageous to implement functions

of a processor in the shortest amount of time possible so results are available as quickly as possible.

Regarding claim 17, Agrawal discloses the despreading code shown in figure 5 has a spreading factor divisible by four.

Regarding claims 18 and 19, Agrawal discloses the despreading code contains code segments comprising real and imaginary bits in figure 4.

Regarding claims 20 and 21, Agrawal discloses the channel bits shown in figures 4A and 4B.

Regarding claim 22-25, Agrawal discloses a method for calculating output data in a digital signal processor (column 16, lines 34-45). The processing units can be implemented with a general purpose or specifically designed processor operated to execute instruction codes that achieve the functions described herein (column 16, lines 40-43). The processing units include multipliers 814 and accumulators 816 (column 16, lines 34-37). The multipliers and accumulators are complex (column 10, lines 56-62). The receiver of figure 7 receives the complex dispreading code and data. The spreading code is discloses in column 7, line 64 to column 8, line 6. Agrawal discloses the despreading code contains code segments comprising real and imaginary bits in figure 4. Agrawal discloses the channel bits shown in figures 4A and 4B.Agrawal does not disclose the complex multiplication, complex addition and storing of the despread result are executed in a single clock cycle of the DSP. However, Catherwood discloses a method for complex multiplication and accumulating a signal (abstract) and executing instructions which operate on data and write the results to an accumulator and write

prior results to memory within a single processor cycle (column 5, line 65 to column 6, line 6). It would have been obvious for one of ordinary skill in the art at the time of the invention to implement the method of Agrawal in the single processor cycle of Catherwood. It is advantageous to implement functions of a processor in the shortest amount of time possible so results are available as quickly as possible.

Regarding claim 26, Agrawal discloses the communication system discussed is a CDMA system that supports voice communication (column 1, lines 15-19). Agrawal discloses the despreading code contains code segments comprising real and imaginary bits in figure 4.

Regarding claim 27, Agrawal discloses a method for processing a signal value in a digital signal processor (column 16, lines 34-45). The processing units can be implemented with a general purpose or specifically designed processor operated to execute instruction codes that achieve the functions described herein (column 16, lines 40-43). The processing units include multipliers 814 (column 16, lines 34-37). The multipliers are complex (column 10, lines 56-62). Agrawal does not disclose the complex multiplication is executed in a single clock cycle of the DSP. However, Catherwood discloses a method for complex multiplication (abstract) and executing instructions which operate on data and write the results to an accumulator and write prior results to memory within a single processor cycle (column 5, line 65 to column 6, line 6). It would have been obvious for one of ordinary skill in the art at the time of the invention to implement the method of Agrawal in the single processor cycle of

Catherwood. It is advantageous to implement functions of a processor in the shortest amount of time possible so results are available as quickly as possible.

Regarding claim 28, Agrawal discloses a method of for processing signal values in a digital signal processor (column 16, lines 34-45). The processing units can be implemented with a general purpose or specifically designed processor operated to execute instruction codes that achieve the functions described herein (column 16, lines 40-43). The processing units include multipliers 814 and accumulators 816 (column 16, lines 34-37). The multipliers and accumulators are complex (column 10, lines 56-62). The receiver of figure 7 receives the complex despreading code and data. The spreading code is discloses in column 7, line 64 to column 8, line 6. Agrawal does not disclose the complex multiplication, complex addition and storing of the despread result are executed in a single clock cycle of the DSP. However, Catherwood discloses a method for complex multiplication and accumulating a signal (abstract) and executing instructions which operate on data and write the results to an accumulator and write prior results to memory within a single processor cycle (column 5, line 65 to column 6, line 6). It would have been obvious for one of ordinary skill in the art at the time of the invention to implement the method of Agrawal in the single processor cycle of Catherwood. It is advantageous to implement functions of a processor in the shortest amount of time possible so results are available as quickly as possible.

Regarding claim 29, Agrawal discloses implementing the method above on numerous fingers in the receiver. This is shown in figures 7 and 8.

Regarding claim 30, Agrawal discloses the despreading code contains code segments comprising real and imaginary bits in figure 4.

Conclusion

Applicant's amendment necessitated the new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin M. Burd whose telephone number is (571) 272-3008. The examiner can normally be reached on Monday - Friday 9 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on (571) 272-3021. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kevin M. Burd
3/3/2006

KEVIN BURD
PRIMARY EXAMINER